

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Steven J. Koester

Examiner: Anh D. Mai

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For: SEMICONDUCTOR FIELD-EFFECT
TRANSISTOR HAVING STRAINED-LAYER
Dated: July 15, 2009

Confirm. No: 7401

Commissioner of Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

SUPPLEMENTAL RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

In response to the Advisory Action dated July 9, 2009 and the Final Office Action dated April 17, 2009, Applicants respectfully request that the following remarks and amendments be considered for entry of record in the above-identified patent application.

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent & Trademark Office via Electronic Filing through the United States Patent and Trademark Office e-business website, on July 15, 2009.

Dated: July 15, 2009


Harry Andrew Hild Jr.